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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,065	06/20/2003	Ming-Huei Shieh	AF01169/AMDP975US	5651

23623 7590 03/23/2005

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EXAMINER	
NGUYEN, DANG T	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 03/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/600,065	SHIEH ET AL.
	Examiner	Art Unit
	Dang T. Nguyen	2824

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/09/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search history*.

DETAILED ACTION

1. This office action is in response to applicant's amendment filed on 01/25/05. Claims 1, 13, 17 and 24 have been amended. Claims 1 – 27 are pending on this application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 - 15, and 17 - 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Le et al. U.S. Patent No. US 6,690,602 B1 - filed Apr. 8, 2002.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding independent claims 1, 17, and 24, Fig. 3 of Lee et al. discloses an architecture that facilitates a reference voltage in a multi-bit memory [302], comprising:

a multi-bit memory core [302] including a plurality of data cells [10] for storing data; first a and second reference arrays [Dynamic Reference A, Dynamic Reference B] of a plurality of multi-bit reference cells [10's of Reference A, 10's of Reference B], the first and second reference arrays fabricated on the memory core (Fig. 3); and a first bit value of a first reference cell (Fig. 4 [414]) of the first reference array (Fig. 4 [Ref A]) averaged with a second bit value of a second reference cell (Fig. 4 [418]) of the second reference array (Fig. 4 [Ref B]) to arrive at the reference voltage (Fig. 4 (A+B)/2) employed and facilitate during a data cell read operation (Col. 4, lines 15 – 17).

Regarding dependent claims 2, 18, and 26, Fig. 3 of Le et al. further discloses comprising a sector [Sector 1] of multi-bit data cells [10] organized in rows and columns with associated word lines [WLs] attached to the multi-bit data cells [10] in a row and with associated bit lines [BLs] attached to the multi-bit data cells [10] in a column, the first and second reference cells [304, 306] forming a multi-bit reference pair (Fig. 4) that is programmed and erased with the multi-bit data cells [10] during programming and erase cycles (Col. 6 lines 7 - 21).

Regarding dependent claims 3 and 19, Fig. 3 of Le et al. discloses wherein the multi-bit reference pair [304, 306] is associated with a word in a word line [WL0], the multi-bit reference pair utilized during reading of bits of the word (Col. 4 lines 15 - 17).

Regarding dependent claims 4 and 20, Fig. 3 of Le et al. discloses wherein the multi-bit reference pair [304, 306] is associated with multi-bit data cells [10s] in a wordline [WL0], the multi-bit reference pair [304, 306] utilized during reading of bits in the wordline (Col. 4 lines 15 – 17).

Regarding dependent claims 5 and 21, Fig. 3 of Le et al. further discloses comprising a plurality of the multi-bit reference pairs [304,306] associated with and attached to a corresponding word line (WL), the associated multi-bit reference pair [304, 306] utilized during reading of bits in the corresponding word line (Col. 4 lines 15 – 17).

Regarding dependent claims 6 and 22, Fig. 3 of Le et al. further discloses comprising the multi-bit reference pair [304,306] is associated with multi-bit data cells [10] in the sector (Sector 1), the multi-bit reference pair [304, 306] utilized during reading of bits in the sector (Col. 4 lines 15 – 17).

Regarding dependent claims 7 and 23, Le et al. discloses wherein the memory core (Fig. 3) including a plurality of data sectors (Col. 5 lines 40 - 42) that are accessible by the first and second reference arrays [304, 306], the first and second reference arrays [304, 306] located the plurality of data sectors (Fig. 3 disclosing multiple sectors separates by a broken lines for each sector, and the broken line on the right side of the Reference B clearly teaches there is at least one more sector which located on the right side of 304 and 306).

Regarding dependent claim 8, Figs. 1–3 of Le et al. discloses an integrated circuit comprising the memory.

Regarding dependent claim 9, Fig. 3 of Le et al. discloses a memory core of computer system.

Regarding dependent claim 10, Fig. 3 of Le et al. discloses an electronic device of memory system.

Regarding dependent claims 11 and 25, Le et al. discloses the first and second reference arrays (Fig. 3 [304, 306]) including corresponding reference cells (Fig. 4 [404, 406]) that are interleaved among the data cells (Fig. 4 [402]).

Regarding dependent claim 12, Fig. 3 of Le et al. discloses a plurality of data sectors (Col. 5 lines 40 - 42) such that each data sector is associated with at least one of the first and second reference array [304, 306] of multi-bit reference cells [10s].

Regarding independent claim 13, (Figs. 3 and 4) of Le et al. disclose an architecture that facilitates a reference voltage (Fig. 4) in a multi-bit memory comprising: a multi-bit memory core (Fig. 3) for storing data, the memory core including two groups (Col. 5 lines 40 – 42) of data sectors (Fig. 3 [10s]); first and second reference arrays (Fig. 3 [304, 306]) of a plurality of multi-bit reference cells (REFERENCE A, B), the first and second reference arrays (Fig. 3 [304, 306]) fabricated on the memory core (Fig. 3) interstitial to the groups (Col. 5 lines 40 – 42) of data sectors (Fig. 3 [10s]); a first bit value (Fig. 4 [404]) of a first reference cell (Fig. 3 [304]) of the first reference array (Fig. 3 [10s of 304]) and a second bit value (Fig. 4 [406]) of a second reference cell (Fig. 3 [306]) of the second reference array (Fig. 3 [10s of 306]) forming a reference pair whose respective bit values are averaged (Fig. 4 [(A+B)/2]) to arrive at the reference voltage for read operation (Col. 4 lines 15-17).

Regarding dependent claim 14, Le et al discloses the groups (Col. 5 lines 40 – 42) of data sectors read in an interleaved manner with a selected reference pair (Fig. 4, Col. 4 lines 15 - 17).

Regarding dependent claim 15, Le et al. discloses wherein the first and second reference arrays precharged before being averaged (Fig. 4) and (Col. 3 lines 8-27).

Claims 13, 16, 24 and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Kurihara et al., U.S. Patent No. US 6,791,880 B1 - filed May 6, 2003.

Regarding independent claims 13 and 24, Figs. 4 and 5 of Kurihara discloses an architecture and a system for providing and facilitating a reference voltage in a multi-bit memory, comprising: a multi-bit memory core for storing data (Col. 1 lines 47-49), the memory core including two groups of data sectors (Fig. 5, Group 1 [I/O: 0, 8, 1, 9, 2, 10, 3, 11] and Group 2 [I/O: 4, 12, 5, 13, 6, 14, 7, 15]); First and second reference array of a plurality of multi-bit reference cells [Ref A and Ref B], the first and second reference arrays fabricated on the memory core interstitial to the groups of data sectors (Fig. 5); and a first bit value of a first reference cell of the first reference array (Fig. 4 [445]) and a second bit value of a second reference cell of the second reference array (Fig. 4 [470]) forming a reference pair whose respective bit values are averaged to arrive at the reference voltage (Fig. 4 [435]) (Col. 5 lines 14-24) for read operation or utilized during a read operation or to facilitate a read operation (Col. 2 lines 25 – 32).

Regarding dependent claims 16 and 27, Fig. 5 of Kurihara discloses a redundancy [525] array located at least one of proximate and adjacent to the groups of data sectors.

Response to Arguments

3. Applicant's arguments filed 09/28/04 have been fully considered but they are not persuasive.

4. With respect to claims 1, 17 and 24, under remarks, applicant argued " Le et al. does not teach or suggest averaging reference bit values during read operation". Examiner is respectful disagrees from the following:

Fig. 4 of Lee et al. '602' as applied to prior office action, clearly discloses an average (A+B)/2 bit values of reference cells (Ref A, Ref B) is arriving at an input terminal of differential amplifier 426; wherein the averaged voltage (A+B)/2 at the input of the differential amplifier is a reference voltage for comparing with the voltage of the memory cell 420 arrived at other input terminal of differential amplifier 426 (See Col. 5 lines 65 – 67) during read operation (Col. 4 lines 15 – 17).

5. Under remarks, with respect to claims 13 and 24, under remarks applicant argued "Kurihara does not teach or suggest averaging reference bit values during read operation". Examiner is respectful disagrees from the following:

Fig. 4 Kurihara et al. as applied to prior office action, clearly discloses a first reference cell of the first reference array (445) and a second bit value of a second reference cell of the second reference array (470) forming a reference pair whose respective bit values (435) are averaged (Col. 5 lines 20 - 24) to arrive at the reference input voltage terminal of the differential amplifier (30) for comparing with the voltage of the memory cell (405) arrived at other input terminal of differential amplifier (430).

Therefore, Le et al. '602' and Kurihara et al. '880' from prior office action are applying to this office action.

Prior art

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Yamada et al.	Pub. No.: US 2003/0206446 A1	Pub. Date: Nov. 6, 2003
Takahashi et al.	Patent No.: US 6,639,849 B2	Date of Patent: Oct. 28, 2003

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

8. Any inquiry concerning this communication from the examiner should be directed to Dang Nguyen, who can be reached by telephone at (571) 272-1955. Normal contact times are M-F, 8:00 AM - 4:30 PM.

Upon an unsuccessful attempt to contact the examiner, the examiner's supervisor, Richard Elms, may be reached at (571) 272-1869.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is (703) 305-3900. The faxed phone number for organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the Status of an application may be obtained from the patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or EBC@uspto.gov.

Dang Nguyen 3/18/2005

VAN THU NGUYEN
PRIMARY EXAMINER